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Design of a 3 GHz Fine Resolution LC DCO

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Design of a 3 GHz Fine Resolution LC DCO

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Dedicated to my family and friends, for their support.

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Abstract

Design of a 3 GHz Fine Resolution LC DCO

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The University of Texas at Austin, 2017

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In this thesis, the design of a fine resolution LC digitally controlled oscillator (DCO) is introduced. Two NMOS varactor banks are used to achieve 12 bits medium and fine frequency tuning. Both delta-sigma modulator and capacitive divider circuit are implemented to achieve a finer resolution and a larger dynamic range. The LC-oscillator has a coarse tuning range from 3.05 GHz to 3.85 GHz and a fine tuning range of 50MHz. It features a phase noise level of -115dBc/Hz at 1MHz frequency offset and consumes 5.4mW. Efficient simulation methodology is explored. Finally, this DCO is simulated in an All-Digital Phase Locked Loop (ADPLL) with other ideal behavior blocks implemented using Verilog-A, and the performance of the DCO is evaluated.

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Chapter 1: Introduction

1.1 MOTIVATION

Phase-Locked Loop (PLL) is widely used in wireless communication system for the purpose of frequency demodulation and frequency synthesis. Charge pump PLL is the most common architecture in RF applications. Unfortunately, the analog PLL is not compatible with digital baseband (DBB) processor, which has migrated to the deep-sub-micron CMOS process [2]. The deep sub-micron CMOS process offers very limited voltage headroom, and makes analog circuit extremely difficult to implement. Therefore, research on All-Digital PLL (ADPLL) is popular recently, which has many advantages compared to the traditional analog PLL. By avoiding analog-intensive blocks, a fully digital design can achieve lower power consumption, less cost and higher reproducibility. The large capacitors and resistors in the loop filter are replaced by the digital loop filter, which significantly reduces the area.

Time-to-digital converter (TDC) and digitally controlled oscillator (DCO) play important roles in the performance of ADPLL. Instead of using a voltage input in voltage controlled oscillator (VCO), the operating frequency of DCO is determined by its digital input words. Two types of oscillator are commonly used in DCO design: LC oscillator and ring oscillator. The frequency tuning of LC oscillator is achieved by changing the capacitance of LC tank, and the tuning of ring oscillator is achieved by changing the bias current of the inverters. Ring oscillator takes much less area and has wider tuning range, however, its noise performance is much worse than LC oscillator. Therefore, most RF

systems use LC oscillator to achieve less phase noise. This thesis also focuses on LC oscillator design.

Wireless application always requires a fine frequency resolution, which is still challenging to achieve in digital circuit. For example, the design of a DCO for GSM applications requires a frequency resolution of few kHz with respect to a tuning range of several hundred MHz around the carrier frequency [7]. This resolution corresponds to a capacitance of the order of atto-Farad, which is impossible by using a unit varactor in current technology. One common method is using a sigma-delta modulator to move the quantization noise to higher frequencies [2]. The rapid switching between different capacitance results in a finer resolution, however, a high switching frequency is necessary, otherwise it may bring more phase noise. Some research papers offer solutions to improve the DCO frequency resolution, such as capacitance divider [5], [6], and capacitive degeneration circuit [7], however, smaller capacitance is more sensitive to mismatches and may introduce non-monotonicity. Moreover, the tuning range is also reduced and the overall dynamic range does not improve. Another approach is the combination of a digital-to-analog converter (DAC) and a hybrid VCO [8]. However, the design of a linear DAC is non-trivial.

The digital-to-frequency conversion performed by DCO is similar to DAC, which converts digital input into voltage or current output. The mismatches of unit varactor in DCO causes non-linearity and non-monotonicity. The dynamic element matching (DEM) method being employed in DACs is also being used in the design of varactor bank in DCO [1]. It shifts the unit-weighted varactor cyclically and moves the noise to out-of-band frequency.

1.2 STRUCTURE OF THESIS

The thesis is organized as follows: Chapter 2 describes the fundamentals of LC oscillator and its phase noise. Chapter 3 presents the implementation of different varactor tuning banks and the techniques used to achieve a fine tuning resolution. Chapter 4 gives the simulation results of the free-running oscillator. Chapter 5 provides the simulation results of the oscillator in an ideal PLL Verilog-A model. Chapter 6 summarizes the work of this thesis and discusses the future research in this area.

Chapter 2: Oscillator Architecture

This chapter discusses the LC oscillator fundamental. Due to the better noise performance, LC oscillator is chosen for the design. The thesis focuses on the implementation of a DCO at 3GHz band. The general performance metrics include phase noise and power.

2.1 LC OSCILLATOR

2.1.1 LC Tank

An LC tank contains an inductor L and a capacitor C, connected in parallel. At a frequency $f_{osc} = 1/(2\pi\sqrt{LC})$, the LC tank resonates and generates an infinite impedance. The realistic inductor has a series resistance, and the quality factor Q is defined as $L\omega/R_s$, which is infinity ideally. The wire diameter and space between winding will affect Q of an inductor, and Q is chosen to be around 10 in this design.

For a narrow frequency range, the circuit is equivalent to its parallel configuration as shown in Figure 2.1. The parallel network has a resistance of

$$R_p = \frac{L^2\omega}{R_s} = Q^2 R_s \tag{2.1}$$

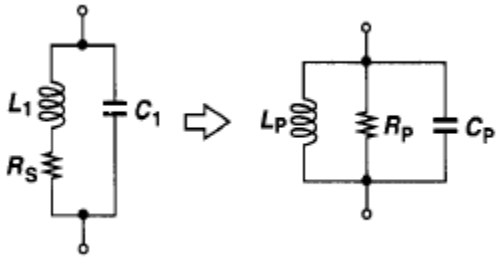

Figure 2.1 Conversion of a tank to parallel components

2.1.2 Crossed-Coupled Oscillator

One of the most popular CMOS implementations is crossed-coupled topology in Figure 2.2, which is also called one-port topology. The passive LC tank provides a decaying oscillatory sinusoidal signal. The active devices compensate the energy lost from inductor's parasitic resistance with a negative resistance.

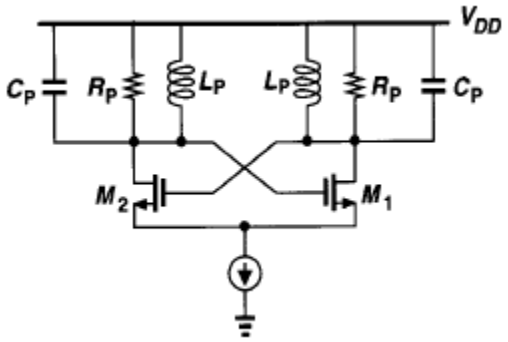

Figure 2.2 Crossed-coupled oscillator topology [10]

The source follower with positive feedback in Figure 2.2 provides a negative input impedance of $-2/g_m$, where g_m is the transconductance of cross coupled pair M1 and M2. Figure 2.3 provides the one-port view of the circuit in Figure 2.2. The negative impedance injects energy into the circuit which compensates the lost in LC tank. The tank remain oscillating only when

$$\frac{1}{g_m} > R_p \tag{2.2}$$

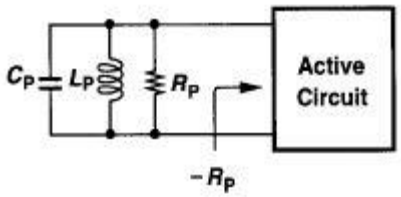

Figure 2.3 One-port view of cross-coupled oscillator

The amplitude of output oscillating signal is given by

$$V_{osc} = I_{tail}R_p \tag{2.3}$$

2.1.3 Proposed Oscillator Architecture

Figure 2.4 shows the oscillator topology used in this design. The circuit in Figure 2.2 has a common mode voltage Vdd, and the output of one node would exceed the supply voltage, which can easily break down the devices. Both NMOS and PMOS being used as cross-coupled pair would give multiple benefits. While adding two device on the top, the oscillation output is within the supply voltage. This structure also helps achieve a better phase noise [9]. Under the same bias current, the oscillating amplitude is doubled by using this topology. Another benefit is that the output common mode level is close to half of the supply voltage.

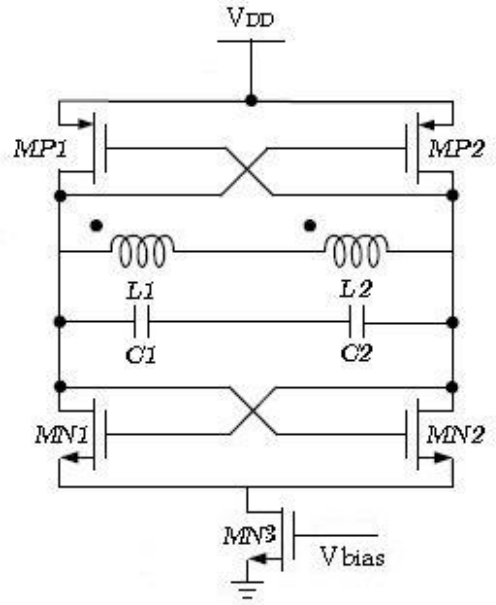

Figure 2.4 Proposed Oscillator Topology

Table 2.1 below gives the parameter of device in Figure 2.4.

Component	Parameter
Inductor	1.75 nH
MN1/MN2	30um/0.18um
MP1/MP2	60um/0.18um
MP3	60um/0.18um
Fixed Capacitor	0.5 pF
Total Capacitor On	1.5 pF
Total Capacitor Off	0.95 pF

Table 2.1: Component values for oscillator

2.2 PHASE NOISE

Phase noise is an important metrics used to evaluate the noise performance of oscillator and PLL. Three part contributes the phase noise of a free running oscillator, parasitic resistance of the LC tank, the active negative impedance, and the current source. The Leeson's formula below calculates the phase noise of an oscillator [4].

$$L(\Delta f) = 10log\left(\frac{2FkT}{P_{sig}}\left(1+\left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\right)\left(1+\frac{\Delta f_{1/f^3}}{|\Delta f|}\right)\right) \tag{2.4}$$

Figure 2.5 shows a typical phase noise profile of a free running oscillator, which can be divided into three sections. The flicker noise dominates the curve in the band close to carrier frequency, which gives a -30dB/dec roll-off. The middle section of the plot follows Leeson's formula, which gives a -20dB/dec roll-off. The flat part is determined by noise factor, temperature and signal power.

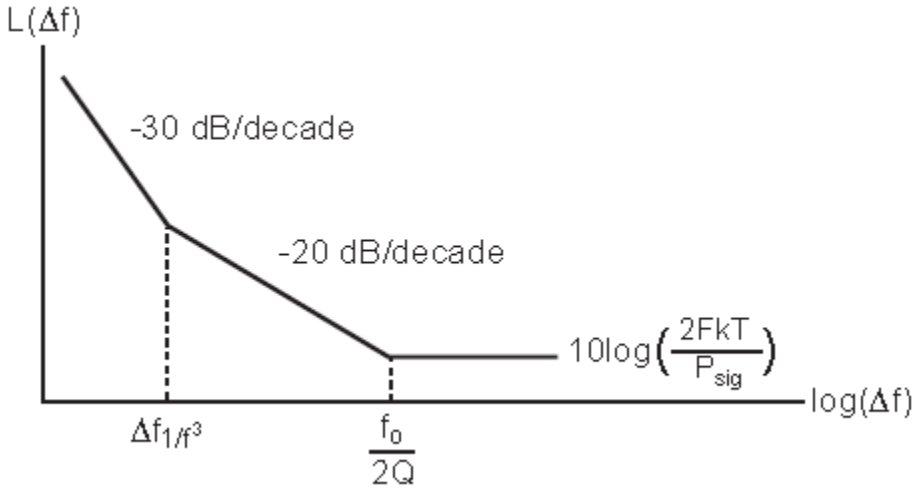

Figure 2.5 Phase noise of a free running oscillator

Chapter 3: Design of Varactor Bank

Although both inductance and capacitance determine the oscillating frequency of an LC oscillator, it is much more practical to fix the inductor while tuning the capacitance. The variable capacitance is implemented by switchable capacitors and NMOS varactors. The whole oscillator contains three tuning banks, coarse tuning bank, medium tuning bank and fine tuning bank, to achieve different frequency tuning steps.

3.1 VARACTOR

Recent DCO designs prefer switched capacitor banks rather than a single varactor. The former one divides the total capacitance into unit varactors, and each varactor only has two possible control voltage, which does not need a DAC to generate analog control signal.

The medium and fine mode tuning are implemented by NMOS transistors as shown in Figure 3.1. The gate of the MOSFET is connected to oscillation nodes. The source and drain are connected together as the other terminal, which is controlled by its digital control input. The gate capacitance is affected by this control voltage and hence tuning of capacitance is achieved.

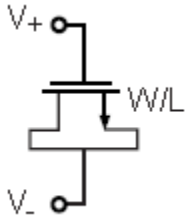

Figure 3.1 A MOS varactor

Figure 3.2 shows the physical structure of a NMOS transistor used as a varactor when the source, drain and substrate are tied together [1]. When positive voltage is applied on the gate, the holes in p-type substrate are repelled and a depletion region is formed under the gate. The gate oxide C_{ox} and the capacitance due to the depletion region C_{delp} are in parallel. This results in a smaller varactor capacitance. When the gate voltage is reduced or negative voltage is applied, the gate attracts a large number of holes and no depletion region is formed. The capacitance reaches maximum, which is equal to C_{ox}.

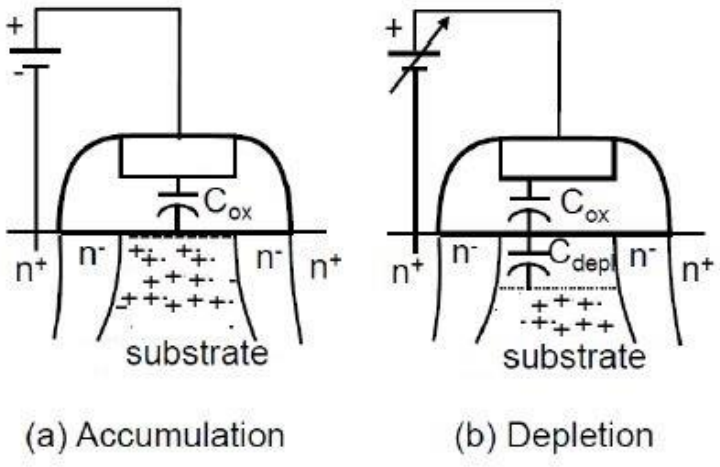

Figure 3.2 Physical structure of a NMOS transistor used as a varactor

Figure 3.3 shows a curve of a NMOS varactor capacitance vs. control voltage (C-V curve) in the simulation with 180nm process model. In deep-submicron process, the linear range of the C-V curve is very narrow. This sharp slop gives a high frequency gain, which is not desired because it will make oscillator very sensitive to the noise of its controlled voltage. Therefore, a MOS varactor only has two working mode, high-capacitance or low-capacitance, depending on its digitally controlled input. The low frequency is obtained if the control voltage is low, and high frequency is obtained if the

control voltage is high. NMOS varactor is chosen due to its well-defined high and low capacitance states.

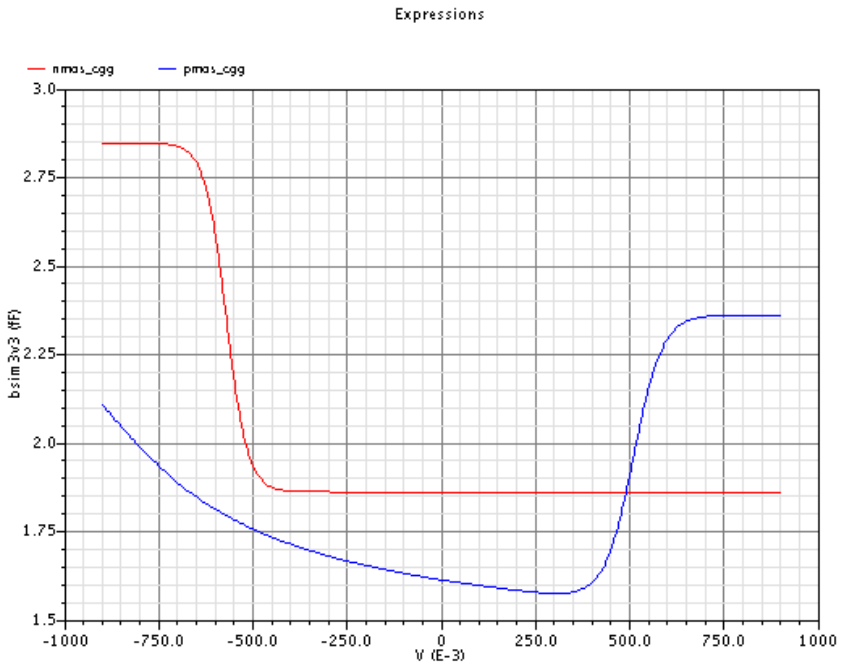

Figure 3.3 Gate capacitance vs. source to gate voltage Vsg of NMOS and PMOS

Each unit varactor can be modelled as shown in Figure 3.4. C_0 represents the low-capacitance state. ΔC represents the capacitance difference between the high and the low capacitance state. Therefore, each varactor can be expressed as a function of its input control voltage as

$$C = C_0 + \overline{D} \cdot \Delta C \tag{3.1}$$

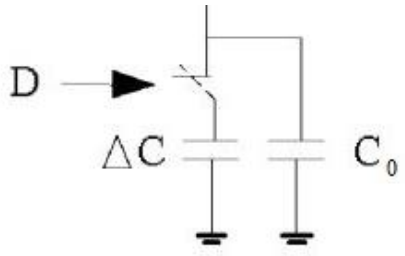

Figure 3.4 Modeling varactor as a switchable capacitor

3.2 Design of Medium and Fine Tuning Bank

Both medium and fine tuning bank are implemented by thermometer coded NMOS varactors. The oscillator operating frequency can be expressed as

$$f = \frac{1}{2\pi\sqrt{L \cdot (C_{fixed} + \sum(C_0 + \overline{D} \cdot \Delta C))}} \tag{3.2}$$

3.2.1 Design of Medium Tuning Bank

The medium tuning bank consists of 6 bits, which was used to control a matrix of 8×8 varactors as shown in Figure 3.5. The varactor matrix is driven by the row and column decoders, which are modeled in Verilog-A. Each varactor is controlled by its row selector, column selector and previous row selector.

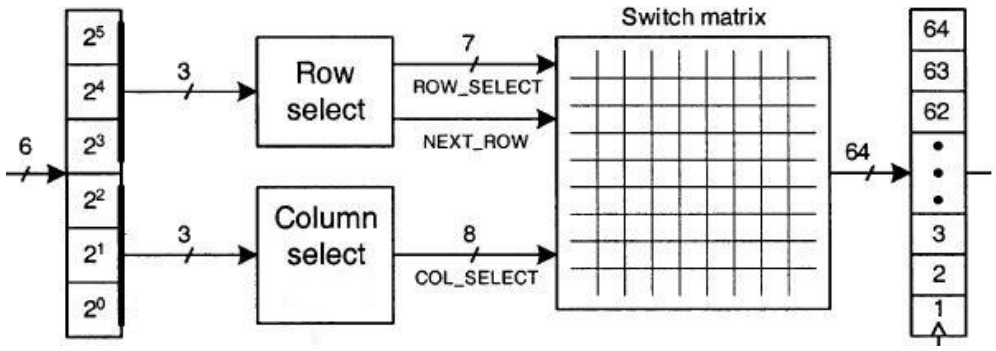

Figure 3.5 Block diagram of medium tuning

3.2.2 Design of Fine Tuning Bank

3.2.2.1 Capacitive Divider

Based on LC oscillator frequency equation 2.1, the frequency tuning step is calculated in equation 3.3. The center frequency of the design is 3GHz. The minimum ΔC can be achieved by the smallest MOS varactor is 0.177fF, which gives a maximum resolution of 17 kHz. The resolution becomes worse with higher oscillation frequency. Other circuit technique should be applied to pursue a finer resolution.

$$\Delta f = 2\pi^2 \cdot L \cdot f^3 \cdot \Delta C \tag{3.3}$$

Capacitance division circuit in figure 3.6 can be used to scale down ΔC and provide a finer tuning resolution [5], [6]. The fine tuning part includes fine tuning MOS varactor, paralleled capacitor C_1 and AC coupling capacitor C_2.

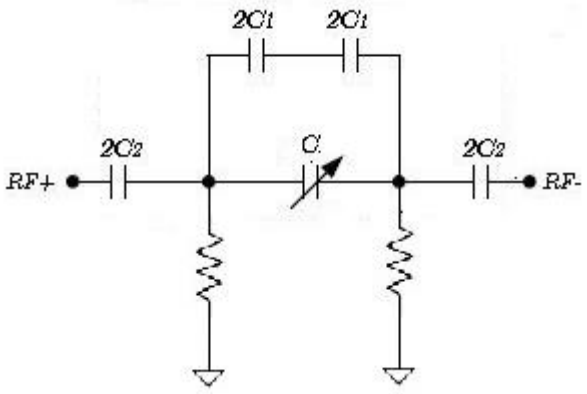

Figure 3.6 Capacitance divider

The equivalent capacitance is calculated in equation 3.4. Capacitor at the center is the NMOS varactor bank, the value of which is determined by the input code. C_1 and C_2 are MOS capacitors that scale the varactor. C is the minimum fixed capacitance of the varactor bank. The equation 3.4 is only valid when $C_1 > C_2 >> C$. Two resistors connect the gate of MOS varactor to the ground to provide a DC bias. The resistance are big enough such that it does not affect the capacitance and the division ratio of the capacitive divider network.

$$\Delta C_{eq} \approx \left(\frac{C_2}{C + C_1 + C_2}\right)^2 \cdot \Delta C \approx \left(\frac{C_2}{C_1}\right)^2 \cdot \Delta C \tag{3.4}$$

3.2.2.2 Time-averaged Dithering with ΔΣ Modulator

A digital ΔΣ modulator would implement a time-averaged dithering to further improve frequency resolution [1]. The structure of the first order digital ΔΣ Modulator is

shown in Figure 3.7. It is clocked by the 800 MHz divided-by-4 oscillator clock. If the DCO is updated at a frequency of 20 MHz, the rough sampling rate is 800MHz/50MHz = 50. It is implemented using Verilog-A code (see Appendix A).

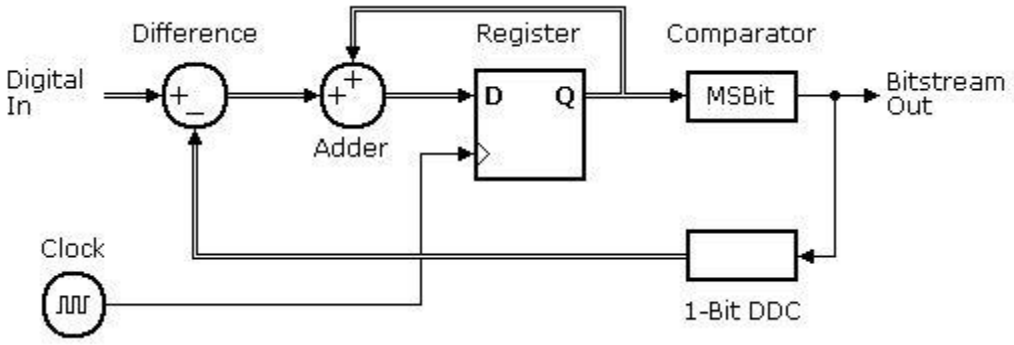

Figure 3.7 Block diagram of a first order digital ΔΣ modulator

The ΔΣ modulator encodes the 6 bit digital input into 4 bit fine tuning control digital code. Quantization error is introduced, which is attenuated at low frequencies and accumulated at high frequencies in this process. The z-domain block diagram and signal transfer function is shown as follow:

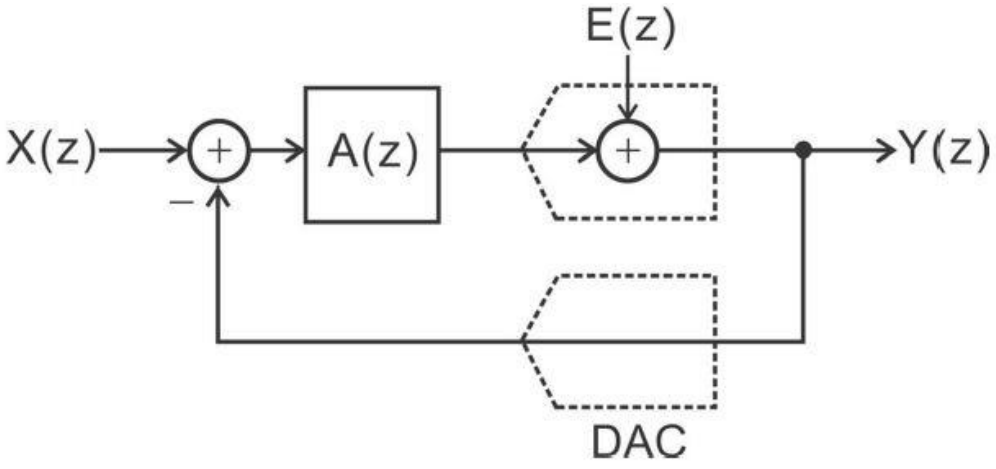

Figure 3.8 z-domain block diagram of a first order digital ΔΣ modulator

$$Y(z) = X(z)\frac{A(z)}{1 + A(z)} + E(z)\frac{1}{1 + A(z)} \tag{3.5}$$

A(z) represents the adder and the register in the digital ΔΣ modulator, which acts as an integrator. Therefore the system passes signal X(z) and high pass filters the quantization error E(z).

3.3 DESIGN OF COARSE TUNING BANK

The NMOS varactor tuning provides a relatively continuous but narrow tuning range. The coarse tuning bank is implemented using 5 bit binary weighted switchable capacitors to give a wide tuning range as shown in Figure 3.8. The medium and fine bank can cover 1 LSB of the coarse bank. The oscillator operating frequency can be expressed as

$$f = \frac{1}{2\pi\sqrt{L \cdot (C_{fixed} + \sum(\overline{D}_k \cdot 2^k \cdot \Delta C))}} \tag{3.6}$$

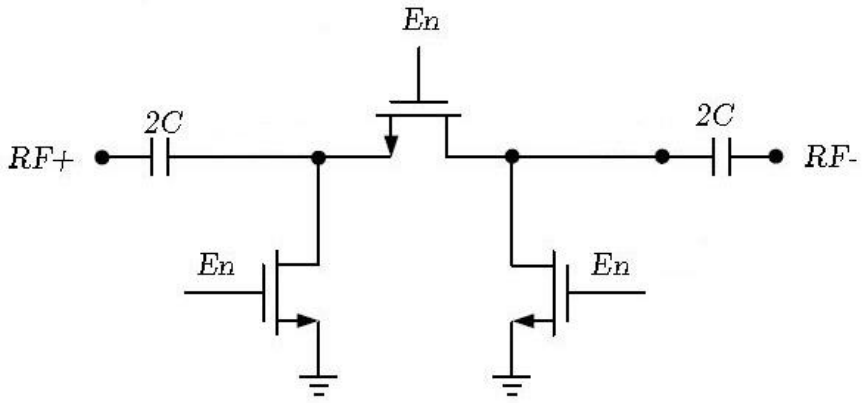

Figure 3.9 Schematic for a unit coarse bank

3.4 Design of Auxiliary Blocks

3.4.1 Design of Differential to Single Ended Converter and Front-end Buffer

The frequency divider requires full swing single ended input, therefore, a differential to single-ended operational amplifier (op-amp) converts oscillator's differential output into a single-ended signal and a front-end buffer amplifies oscillator's output into full swing as shown in Figure 3.9. A simple inverter is used to implement the buffer. The differential to single-ended converter has a high DC gain, which may shift the signal above or below the inverter threshold voltage. To solve this problem, another buffer is added between the input and output of the inverter [11]. Only one of PMOS or NMOS will be turned on and act like source follower, which will shift the input in a direction opposite to the output.

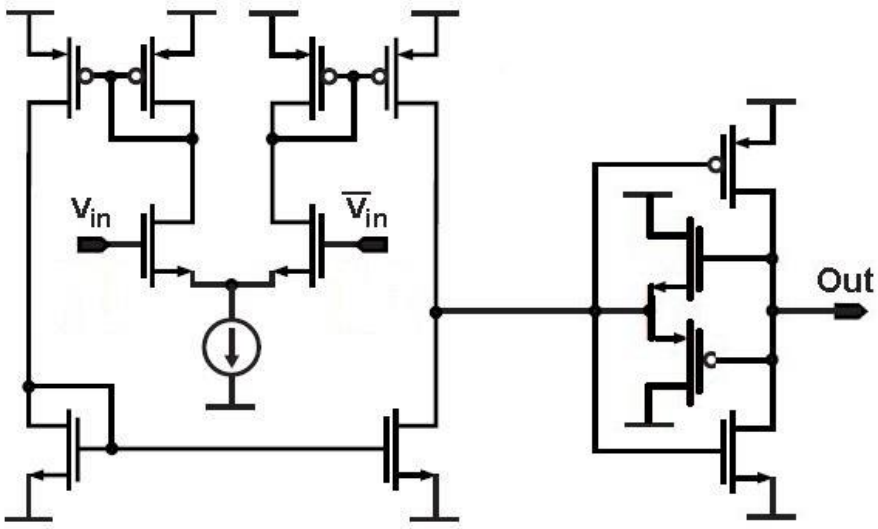

Figure 3.10 Differential to Single Ended Converter [11]

3.4.2 Design of Frequency Divider

A high speed frequency divider is required to divide the oscillator output by 4, which is directly sent to ΔΣ modulator, retiming circuit and the counter in PLL's feedback loop. The dynamic true-single-phase-clock (TSPC) architecture in Figure 3.10 is used in this design, which has advantage of no static power dissipation and relatively fast speed.

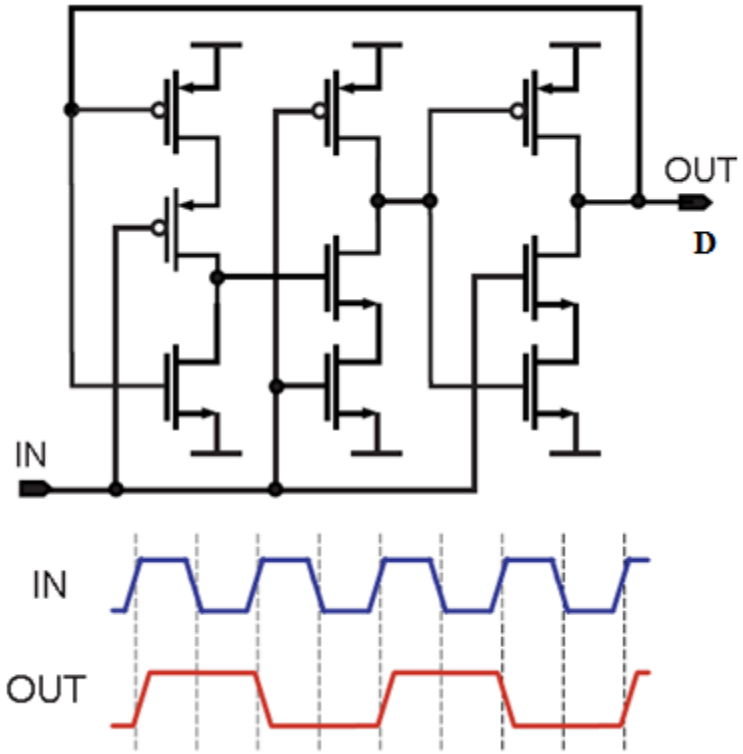

Figure 3.11 Implementation of divide-by-2 frequency divider [11]

When input clock IN is low, the first stage operates as an inverter and the second stage is disabled. After IN goes from low to high, the first stage is disabled and the output retains its value $\bar{D}$. Both of the second stage and the third stage are enabled and operate as inverters, which pass $\bar{D}$ to the output and flip the input of the first stage. After IN goes to

low again, the second and third stage are both disabled and the output retains its value. Thus, the output flips only when IN rises.

3.5 SUMMARY

Figure 3.11 shows the oscillator topology and the implementation of varactor banks.

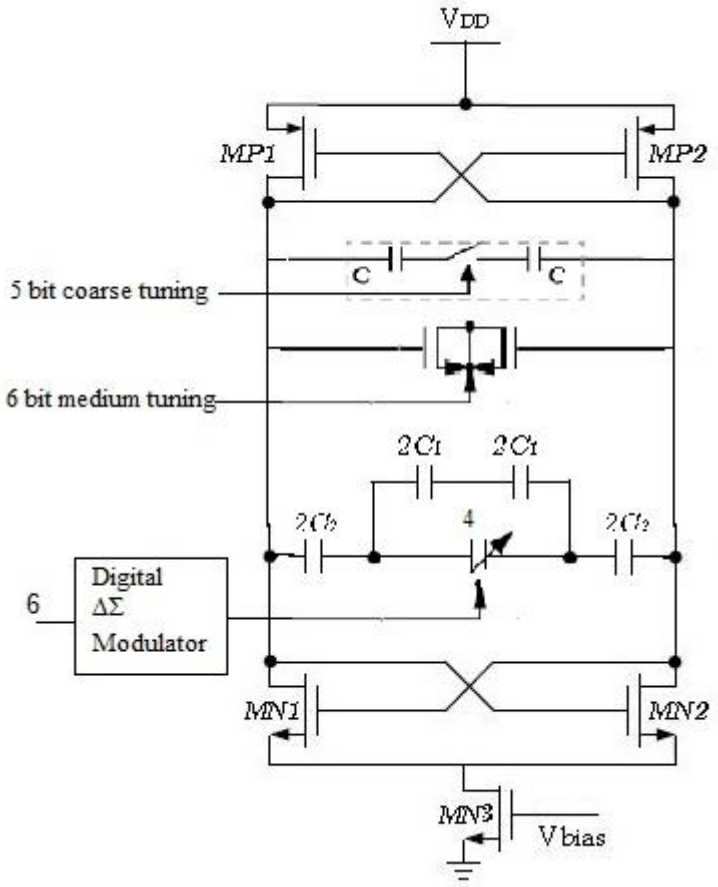

Figure 3.12 Implementation of varactor banks

The value of switchable capacitors and the varactors are listed in Table 3.1. The capacitance in the implementation is smaller than the calculated value, for the reason that NMOS and PMOS cross-coupled pairs also contribute to the total capacitance. More detailed parameters are listed in Table 3.2.

Tuning bank	Component	Parameter
coarse	unit switchable capacitor	40 fF
medium	varactor	180nm/1.44um
fine	varactor	180nm/1.44um
	C1	600 fF
	C2	150 fF
	R	1 MΩ
other	fixed capacitor	0.5 pF

Table 3.1: Component values for capacitor banks

Tuning bank	C_{off}	C_{on}	ΔC	$\Sigma(\Delta C)$
coarse	0	20 fF	20 fF	0.62pF
medium	2.05 fF	1.34 fF	0.71 fF	44.73 fF
fine	0.128 fF	0.084 fF	0.044 fF	0.66 fF

Table 3.2: List of parameter for the unit varactor

Chapter 4: DCO Simulation Results

The detailed implementation of the proposed DCO is given in chapter 2 and 3. The proposed circuits were designed in TSMC 0.18μm CMOS process using Cadence tools as a proof of concept. The circuits were simulated using Spectre. Transient and phase noise simulation were performed to evaluate the DCO design.

4.1 Simulation Methodology

The spectrum of oscillator's output was obtained by running transient simulation and performing discrete Fourier transform (DFT) using Cadence built-in DFT function. To observe a frequency resolution of 1 kHz, the transient simulation needs to be at least 1ms, which is very time-consuming. For this reason, the DCO was designed to achieve a frequency resolution of 10 kHz, whose simulation time was acceptable. Higher resolution might be achievable regardless of this simulation time limitation.

The output signal oscillated at a frequency above 3 GHz. In this case, it was necessary to sample the output at a frequency of at least 6 GHz. The number of point could be a few million if the simulation time was long. Figure 4.1 shows the Verilog-A block being used to solve this problem. The oscillator output was multiplied by a sinusoidal wave close to the oscillating frequency, which performed down-conversion of output to baseband. Then, a low-pass filter followed to avoid aliasing. This block gave an output of a few megahertz, which is much easier for DFT analysis.

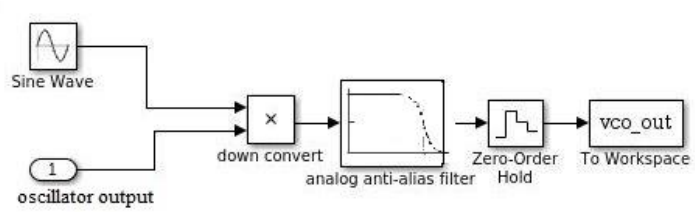

Figure 4.1 Block diagram to down convert output signal to baseband

4.2 SIMULATION RESULTS

The coarse tuning curve is shown in Figure 4.2. The design achieved a tuning range from 3.05 GHz to 3.85 GHz with a coarse tuning step of 25 MHz. The transient simulation result at a frequency of 3.05 GHz is shown in Figure 4.3. It took a few cycles for the oscillator to start up, and it reached a peak-to-peak amplitude of 1.5V. The frequency divider divided the DCO output by 4.

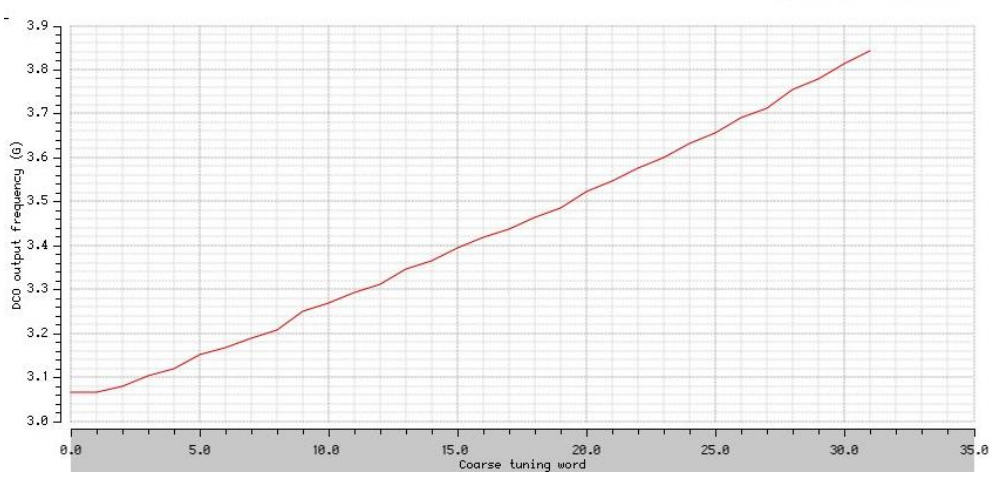

Figure 4.2 Coarse tuning curve

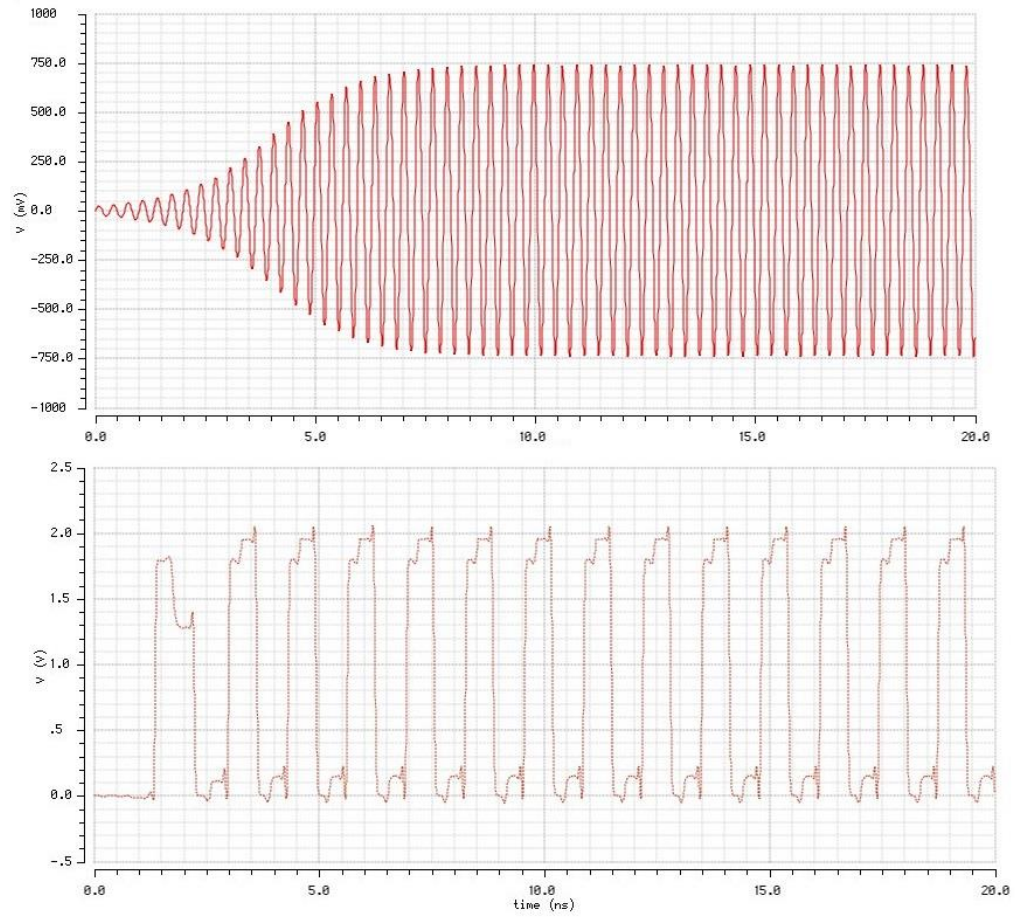

Figure 4.3 Transient simulation results of DCO and frequency divider output

Figure 4.4 and 4.5 describes the DFT plot of the down-converted DCO output at a frequency of 3.056GHz. The LSB of the fine tuning bank provided a frequency resolution of 50 kHz.

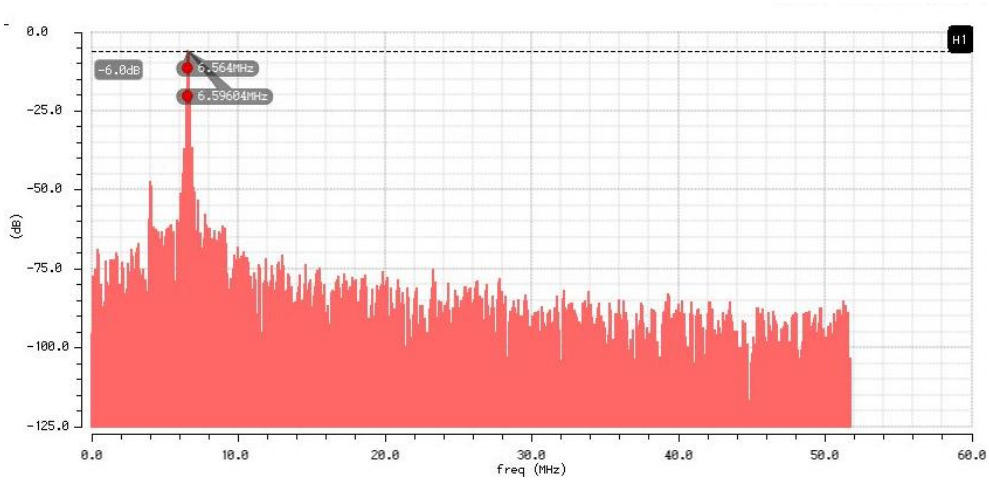

Figure 4.4 DFT plot of down-converted output with a fine tuning word of 0000

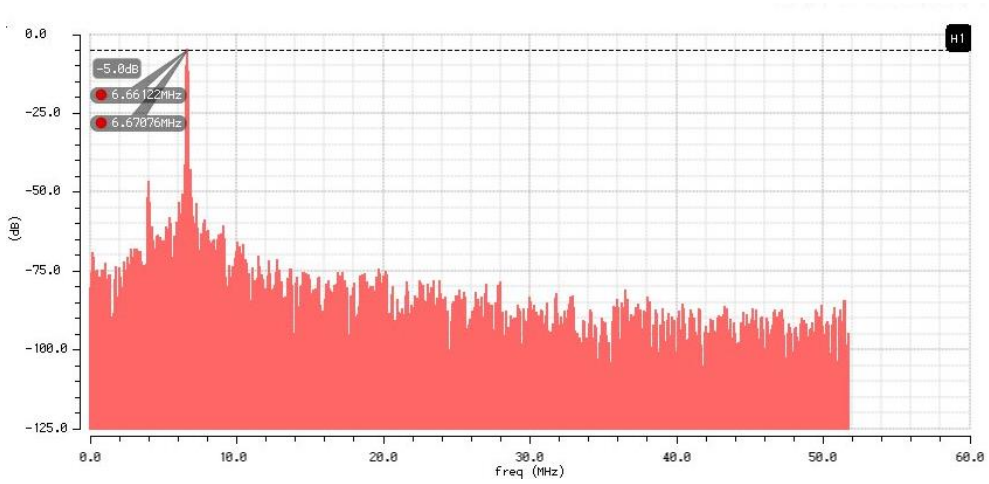

Figure 4.5 DFT plot of down-converted output with a fine tuning word of 0001

Phase noise was measured by running PSS and Pnoise simulation as shown in Figure 4.6. The results matched the Leeson's formula. The higher oscillating frequency gave a worse phase noise profile.

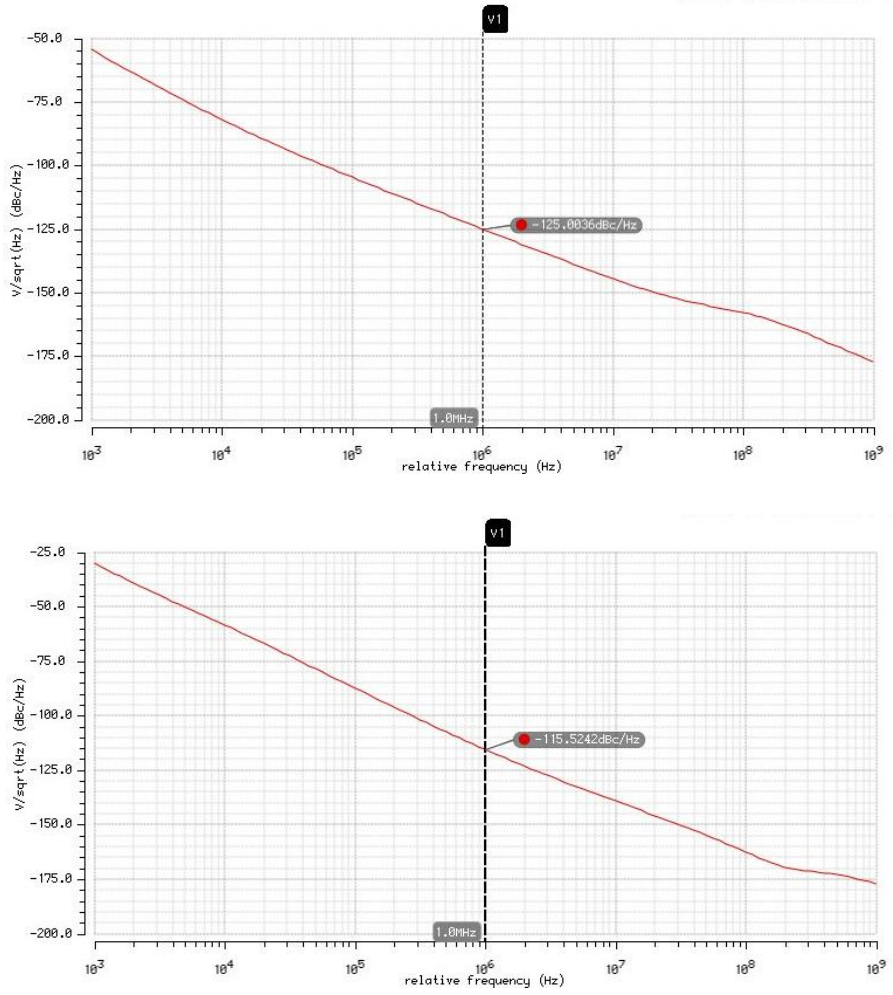

Figure 4.6 Phase noise plot at f = 3.05 GHz and f = 3.85 GHz

Table 4.1 summarizes the performance of the DCO in simulation. The proposed DCO has a voltage supply of 1.8V with a bias current of 3mA. It achieves a tuning range

from 3 GHz to 3.8 GHz with a frequency resolution of 50 kHz. Unfortunately, the implementation of DSM should enable the DCO to reach a resolution of 10kHz, which was not detected finally. The phase noise at 1MHz away from the carrier frequency is -115 dBc/Hz at 3.85 GHz. The figure of merit (FOM) is developed to compare the performance of oscillators, which is defined in equation (4.1).

$$FOM = 20\log\left(\frac{fc}{\Delta f}\right) - PN - 10\log\left(\frac{Power}{1mW}\right) \quad (4.1)$$

Technology	0.18μm
Voltage Supply	1.8V
Current Consumption	3mA
Tuning Range	3.05 GHz – 3.85 GHz
Medium and Fine Tuning Range	50 MHz (12 bits)
Fine Frequency Resolution	50 kHz
Phase Noise @ 1MHz	-115 dBc/Hz
FOM @ 3.8 GHz	179 dB

Table 4.1: Performance summary

Chapter 5: DCO Simulation in Ideal ADPLL Model

A PLL is a negative feedback loop that synchronizes the output signal from oscillator with a reference signal in both frequency and phase. The loop is locked when the phase error between the output signal and reference signal does not change with time. This chapter gives the basic architecture of ADPLL and the Verilog-A modeling of each blocks. The DCO described in previous chapters was simulated within an ideal ADPLL model, and the result is presented in the end.

5.1 ADPLL Architecture

The block diagram of the ideal ADPLL model is shown in Figure 5.1. The time-to-digital converter (TDC) compares the phase of reference input signal with the phase of divided output signal, then digitizes the phase difference between the two signals. The loop filter suppresses the high frequency component produced in TDC and smoothens frequency tuning signal of DCO. This tuning signal controls the frequency of the DCO. The feedback loop divides the oscillator's output and feeds it back to TDC. The performance of the overall PLL is highly depend on the DCO.

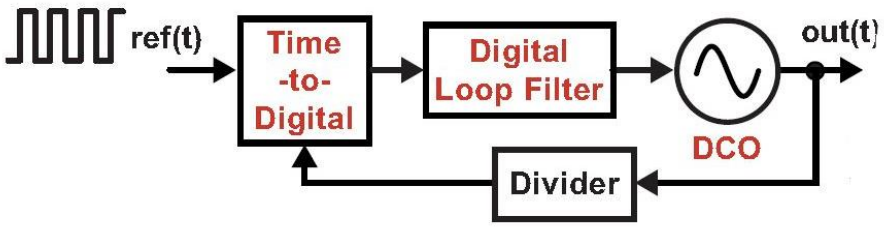

Figure 5.1 Architecture of ADPLL

5.2 MODELING OF BASIC BUILDING BLOCKS

Figure 5.2 shows the frequency domain model of ADPLL. Both loop filter and DCO are updated by reference clock. TDC replaces the phase-frequency detector (PFD) and the charge pump in the traditional analog PLL.

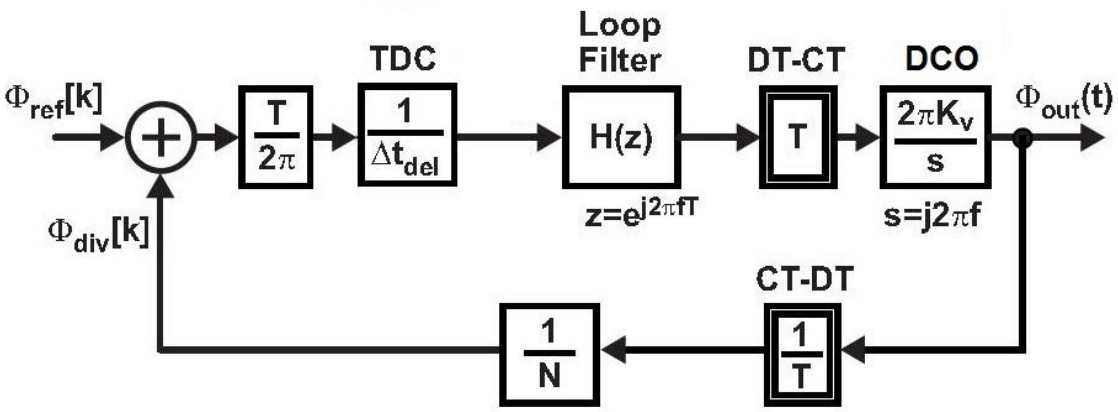

Figure 5.2 Frequency domain model of ADPLL

The TDC first translates the phase difference into time difference, and then digitize the time information. Its s-domain transfer function is given by

$$K_{TDC} = \frac{T_{ref}}{2\pi} * \frac{1}{\Delta t_{del}} \tag{5.1}$$

Where Tref represents the period of reference clock, and Δt_{del} represents the minimum detectable time of TDC.

The digital loop filter has the same function as the analog filter in traditional PLL, whose z domain transfer function can be converted to s domain transfer function. The simple first order infinite response (IIR) filter is popular to implement the loop filter, which has a pole at DC and another zero. Its overall transfer function can be divided into two path, an integral path and a gain path. Since the bandwidth of the PLL loop is usually less

than one tenth of the reference frequency, bilinear transformation can map the z-domain variable into s-domain. The s-domain transfer function is given by

$$H(s) = \frac{\alpha + \beta s T_{ref}}{s T_{ref}} \tag{5.2}$$

The phase error is filtered by the loop filter. The DCO performs digital-to-frequency conversion, which has a gain of its frequency resolution. Since frequency is the derivative of the phase in time domain, the DCO's transfer function can be expressed as:

$$K_{DCO}(\mathrm{s}) = \frac{2\pi K_v}{s} \tag{5.3}$$

The gain of frequency divider is the inverse of its frequency division ratio N between output clock and input clock.

The overall loop gain and the close loop gain is given by

$$T(s) = \frac{4K_v}{T_{del}} \frac{\alpha + \beta s T_{ref}}{s^2} \frac{1}{N} \tag{5.4}$$

$$G(s) = \frac{T(s)}{1 + T(s)} \tag{5.5}$$

5.3 DCO-REFERRED NOISE

The phase noise of oscillator dominates the PLL's high frequency noise, therefore, LC oscillator which produces low phase noise is preferred in RF system. The noise transfer function of DCO is given by

$$\frac{\varphi_{out}}{\varphi_{in}} = \frac{1}{1 + T(s)} = 1 - G(s) \tag{5.6}$$

The low resolution of a DCO introduces quantization error as well. The noise transfer function is given by

$$\frac{\varphi_{out}}{\varphi_{in}} = \frac{\frac{2\pi K_v}{s}}{1+T(s)} = \frac{2\pi K_v}{s}(1-G(s)) \tag{5.7}$$

Figure 5.3 shows the transfer function of two types of noise.

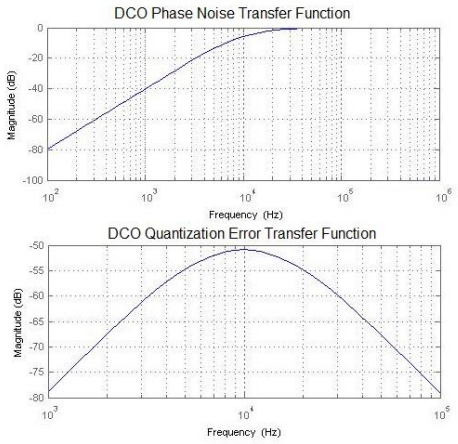

Figure 5.3 Transfer function of DCO Phase Noise and Input Quantization Error

5.4 Simulation Results

To verify the proposed design, the DCO was simulated in an ADPLL. All other building blocks, including TDC, loop filter and frequency divider, are ideal behavior models and implemented using Verilog-A (see Appendix B). The division ratio is 72 and the bandwidth was one fortieth of the reference frequency. The loop was tested with a 50 MHz reference clock. The bode plot of the loop gain is shown in Figure 5.4. The transient simulation plot is shown in Figure 5.5, and its DFT analysis result is shown in Figure 5.6. A few spurs show up in Figure 5.5, which was caused by capacitance change of the LC

tank. The change of capacitance may happens at the moment when oscillating energy is fully stored in one varactor. The preserved charge causes perturbations on oscillating nodes and introduces time jitter. One possible solution to reduce this dynamic error is adding a retiming register in front of DCO [1]. The retiming circuit always changes the capacitance at the moments when there is no charge across the capacitors.

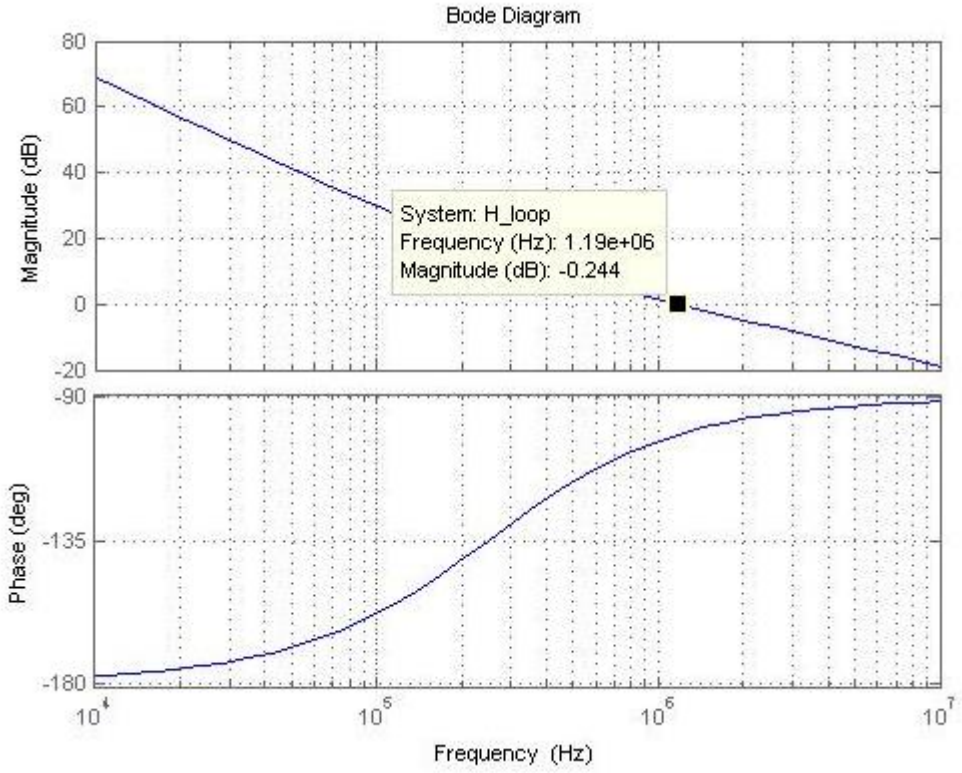

Figure 5.4 ADPLL loop gain bode plot

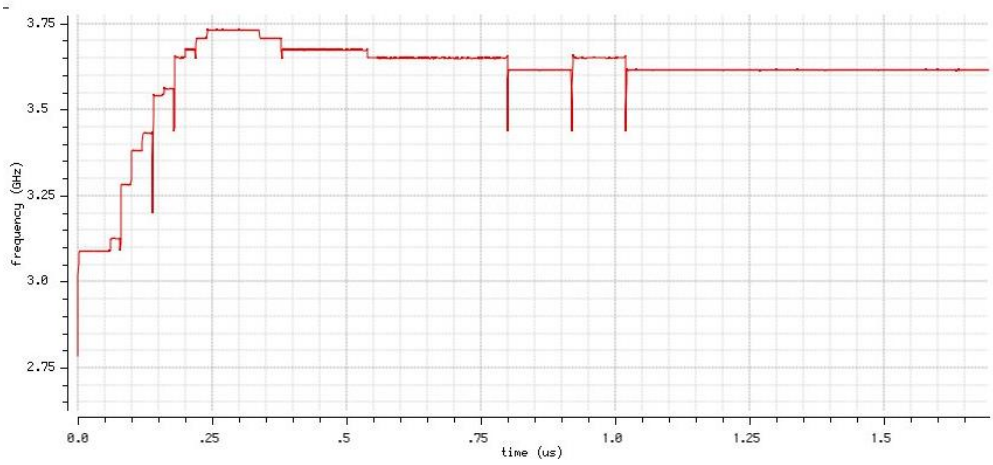

Figure 5.5 Lock transient of ADPLL model

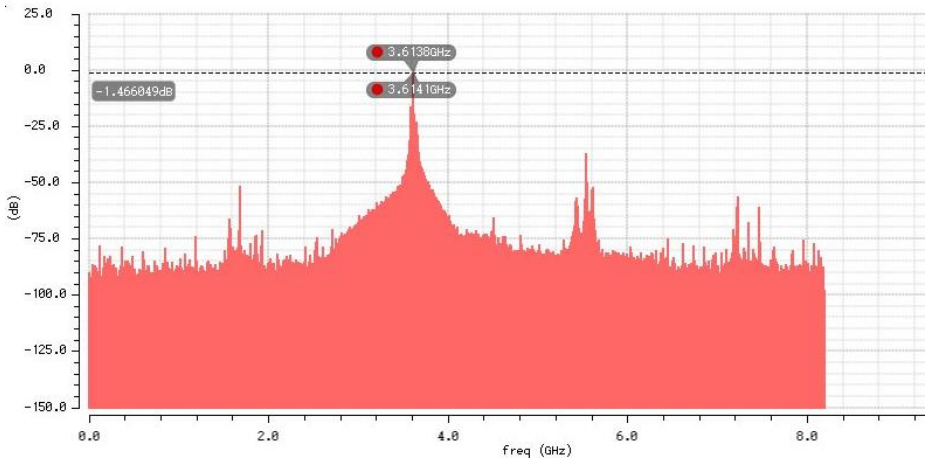

Figure 5.6 DFT plot of DCO output

Chapter 6: Conclusion

6.1 Contribution of This Work

This thesis provides a guideline to the basic LC oscillator design and the implementation of DCO's varactor banks. A DCO is presented in 180nm CMOS process. Fine resolution and wide tuning range are achieved by both making a custom design of capacitor banks and investigating the methods to shrink capacitance in LC tank. It combines two approaches, capacitive divider network and sigma-delta modulator, to improve the resolution. The DCO realizes a decent phase noise performance with a relatively low current consumption.

Simulation methodology is also explored in this thesis. Before performing DFT function, the Verilog-A blocks is used to analyze output such that it spends less simulation time to obtain accurate results. Finally, the thesis presents a method to simulate the DCO in an ideal PLL model to verify the design.

6.2 Future Work

There is much room for optimization. The mismatches in varactor banks play an important role in non-linearity and non-monotonicity of DCO operation. Among dynamic element matching (DEM) methods, data weighted averaging (DWA) is the most efficient one to perform the noise shaping. Besides, the first order $\Delta\Sigma$ modulator in the design generates spurs, which can be replaced by a higher order $\Delta\Sigma$ modulator in the future.

Due to the limited time, the circuit was only verified in schematic simulation. One necessary work is to draw the layout and tape-out the circuit. It is much easier to observe the accurate phase noise plot and frequency tuning characteristic by testing the circuit on silicon.

In addition, the simulation of oscillator is not very accurate and time-consuming. A more efficient simulation methodology need to be investigated to achieve a better design. Other simulators, such as ams, are also options to run the simulation.

Appendix A: Verilog-A Model of ΔΣ Modulator

```
module dsm(in,clk,vout);

        input in,clk;
        output vout;
        electrical in,clk, vout;
        parameter real vdd = 1.8;

        integer vdiff,vsum,vreg;
        integer out;

analog begin
        @(initial_step) begin
        vreg = 0;
        vdiff = 0;
        vsum = 0;
        out = 0;
end

@(cross(V(clk)-0.8,1)) begin
        vdiff = V(in)-V(vout)*4;
        vsum = vreg+vdiff;
        vreg = vsum;
        out = vsum/4;
end

V(vout) <+ transition(out,0,40p);

end
endmodule
```

Appendix B: Verilog-A Model of PLL

(B-1) TDC

```
module TDC(clk_ref,clk_fb,Dout);
        input clk_ref,clk_fb;
        output Dout;
        electrical clk_ref,clk_fb,Dout;
        parameter real vtran = 1;
        parameter real scalar = 0 from [0:inf);
        parameter real range = 50n from [0:inf);
        real t_pre;
        integer flag_ref,flag_fb;
        real T;

    analog begin
        @(initial_step) begin
                flag_ref = 0;
                flag_fb = 0;
        end

        @(cross(V(clk_ref)-vtran,+1)) begin
                if((flag_fb) == 1) begin
                        T = -($abstime - t_pre);
                        flag_ref = 0;
                        flag_fb = 0;
                        if(T < (0-range)) begin
                                T = -range;
                        end
                end
                else begin
                        t_pre = $abstime;
                        flag_ref = 1;
                end
        end

        @(cross(V(clk_fb)-vtran,+1)) begin
                if((flag_ref) == 1) begin
                        T = $abstime - t_pre;
                        flag_ref = 0;
                        flag_fb = 0;
```

```
                        if(T > range) begin
                                T = range;
                        end
                end
                else begin
                        t_pre = $abstime;
                        flag_fb = 1;
                end
        end

        V(Dout) <+ transition(T*scalar);
        end
endmodule
```

(B-2) Loop filter

```
module filter(in,out,clk);
        input in,clk;
        output out;
        electrical in,out,clk;
        real dco_code;
        parameter vtran = 1;
        parameter norm = 100 from [0:inf);
        real inp,inp_pre;

        analog begin
                @(initial_step) begin
                        dco_code = 0;
                        inp_pre = 0;
                        inp = 0;
                end

                @(cross(V(clk)-vtran,+1)) begin
                        inp = V(in);
                        dco_code = dco_code + (8*inp + 256*(inp - inp_pre))/norm;
                        inp_pre = inp;
                end

        V(out) <+ transition(dco_code);
end
endmodule
```

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